

NASA TECHNICAL NOTE



NASA TN D-8509

NASA TN D-8509

AN INTEGRATED CIRCUIT FLOATING POINT ACCUMULATOR

Theodore C. Goldsmith

*Goddard Space Flight Center
Greenbelt, Md. 20771*

1 Report No TND-8509		2 Government Accession No		3 Recipient's Catalog No	
4 Title and Subtitle An Integrated Circuit Floating Point Accumulator				5 Report Date June 1977	
				6 Performing Organization Code 724	
7 Author(s) Theodore C. Goldsmith				8 Performing Organization Report No G-7702 F12	
9 Performing Organization Name and Address Goddard Space Flight Center Greenbelt, Maryland 20771				10 Work Unit No. 862-11-01	
				11 Contract or Grant No	
12 Sponsoring Agency Name and Address National Aeronautics and Space Administration Washington, D.C. 20546				13 Type of Report and Period Covered Technical Note	
				14 Sponsoring Agency Code	
15 Supplementary Notes					
16 Abstract Many scientific instruments flown on spacecraft perform the functions of counting the rates at which different events take place, temporarily storing the accumulated data, and then transmitting the data to the spacecraft telemetry system. In some cases, it is also important to compress the bits required for transmission to conserve telemetry space. Goddard Space Flight Center has developed a large-scale integrated circuit (Type 623) which can perform pulse counting, storage, floating point compression, and serial transmission, using a single monolithic device. Counts of 27 or 19 bits can be converted to transmitted values of 12 or 8 bits respectively. Use of the 623 has resulted in substantial savings in weight, volume, and dollar resources on at least 11 scientific instruments to be flown on 4 NASA spacecraft. The design, construction, operation, and application of the 623 are described.					
17 Key Words (Selected by Author(s)) Accumulators, Integrated circuit				18 Distribution Statement Unclassified—Unlimited Cat. 88	
19 Security Classif. (of this report) Unclassified		20 Security Classif. (of this page) Unclassified		22 Price* \$3.50	
				21 No. of Pages 23	

All measurement values are expressed in the International System of Units (SI) in accordance with NASA Policy Directive 2220.4, paragraph 4.

CONTENTS

	<i>page</i>
INTRODUCTION	1
GENERAL DESCRIPTION	3
GSFC PMOS PROCESS	5
USER INTERFACE INFORMATION	5
DATA CONVERSION ALGORITHMS	7
CIRCUIT OPERATION ANALYSIS	9
Device Physics	9
Cell Descriptions	10
Sequence of Operations	10
Radiation Resistance	15
CONCLUSION	16
REFERENCE	17
APPENDIX A	A-1
APPENDIX B	B-1
APPENDIX C	C-1

AN INTEGRATED CIRCUIT FLOATING POINT ACCUMULATOR

Theodore C. Goldsmith
Goddard Space Flight Center
Greenbelt, Maryland

INTRODUCTION

The Goddard Space Flight Center (GSFC) of the National Aeronautics and Space Administration (NASA) is responsible for the development and flight of a number of scientific instruments flown on spacecraft which involve event-counting in the measurement of charged particles, gamma rays, and other physical phenomena. In such an instrument, there are typically a number of logically different events which can occur. The instrument usually has a number of different detectors or detector elements from which pulses must be accumulated separately. It may be necessary, for example, to distinguish between particles arriving from different directions, or particles with differing energies. As a result, it may be desirable for a single instrument to separately and independently count as many as 64 different pulse signals simultaneously. In some cases, the exact count of events occurring in a known interval is the desired information to be telemetered. However, it is also frequently true that because of the random nature of the subject events, the exact count has little more statistical significance than a truncated or compressed value, which would have the advantage of requiring less telemetry transmission space. In such cases, a device known variously as a floating point accumulator or logarithmic compressor is used. This device converts the exact-count information into a truncated count value and an exponent in such a way that the maximum percentage error between the actual count and the telemetered value is kept fairly uniform regardless of count value.

Because of the relatively large number of floating point accumulators needed, the International Sun-Earth Explorer (ISEE) Project at NASA/GSFC commissioned development of a custom large-scale integrated (LSI) circuit to perform this function. Each LSI circuit would replace up to ten small- and medium-scale integrated circuits, resulting in substantial savings in cost, weight, and volume. The circuit was developed by GSFC and is known as the Type 623 Floating Point Processor (figure 1).

The 623 is designed to accumulate a pulse count of up to 27 bits (1.3×10^8 pulses), convert it to a floating point value of 12, 10, or 9 bits (user option), and provide for serial data interface to a typical spacecraft telemetry system. A fourth mode allows conversion of 19 bits (5×10^5 pulses) to 8 bits.

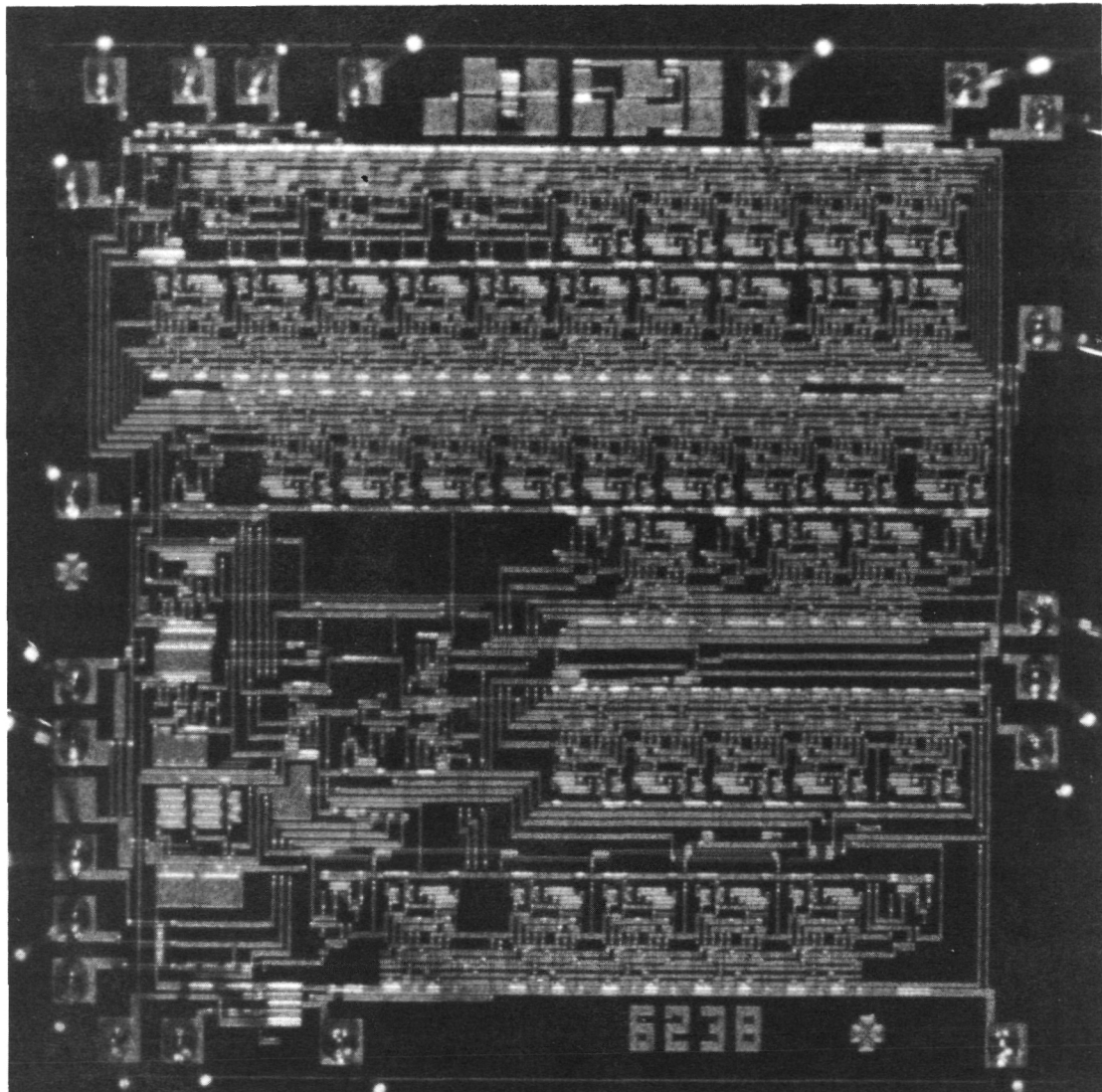


Figure 1. Type 623 floating point processor.

GENERAL DESCRIPTION

The Type 623C microcircuit is a monolithic, P-channel metal oxide semi-conductor (PMOS) device, packaged in a 22-lead flatpack. As shown in figure 2, the circuit consists of input pulse-gating logic, a 27-bit counter (and shift register), A, a 7-bit shift register, X, a 5-bit counter-shift register, Y, and assorted floating point conversion logic. Input pulses are accumulated in counter A. (The input-pulse-gating logic may be used to inhibit counting in applications where several 623 circuits are accumulating pulses from the same source, but during different time regimes. This is typically used to differentiate arrival direction when using a rotating or scanning detector.) At the end of the counting interval a "convert" pulse is applied to pin 15. At this time, further counting is inhibited and a floating-point conversion is performed in which the most significant bits of the number in A are shifted to the X register, and an exponent is placed in the Y register. The counter is then reset at the end of the "convert" pulse and a new counting interval may be begun. The floating point value is available in the X and Y registers to be shifted out serially to the telemetry system as required.

In an ideal case, the original count N would be expressed simply

$$N = X \cdot 2^Y$$

But, because of the particular mechanics used to implement conversion in the 623, its re-conversion algorithm is considerably more complex. The 623 has the capability of converting counts to floating point values in four different formats as described in table 1. For example, a count not exceeding 27 bits may be converted to a 12-bit result in which 7 bits represent the truncated count X, and 5 bits the exponent Y.

Table 1
Type 623 Conversion Modes

Maximum Count Size (bits)	27	27	27	19
Bits in Result	12	10	9	8
Bits in Y	5	5	5	4
Bits in X	7	5	4	4
Mode Control Voltages:				
M19	+	+	+	—
J	—	+	+	+
K	—	—	+	+

A serial data input pin is provided so that a number of 623 parts may be connected in series. A tri-state type output is also provided, so that strings of 623 parts may be multiplexed using a common connection at pin 22.

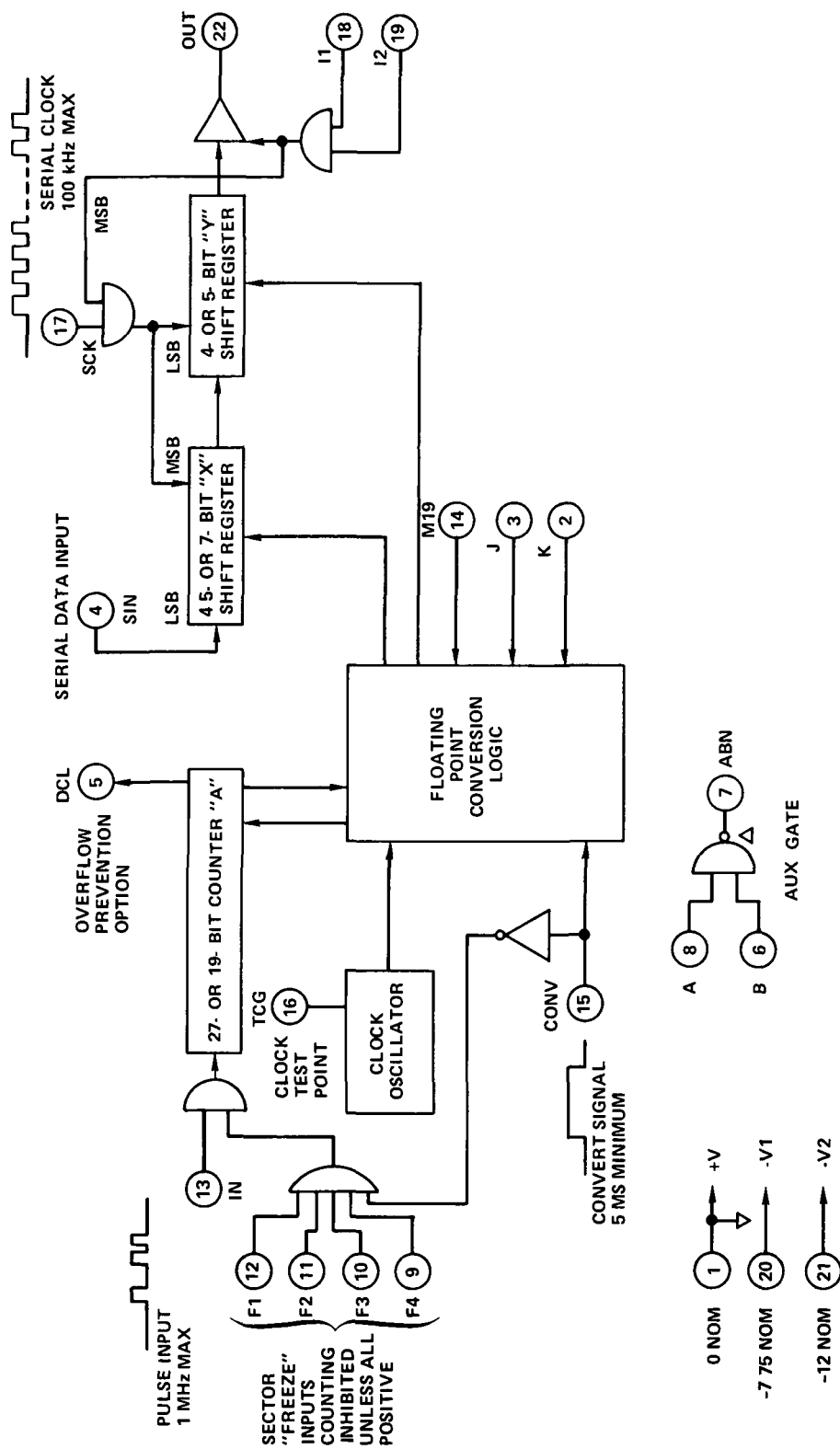


Figure 2. Type 623 floating point processor, block diagram.

GSFC PMOS PROCESS

GSFC has had a pilot production capability for P-channel MOS circuits since 1969, and has produced experimental and prototype circuits on a very low volume basis. GSFC has produced approximately 80 different types of circuits for satellite projects such as the Orbiting Solar Observatory, the High Energy Astrophysics Observatory, and the International Ultraviolet Explorer. The 623 alone is in use on 11 different experiments to be flown on International Sun-Earth Explorers (3 spacecraft) and on TIROS-N. The GSFC process is compatible with that used by several industry sources, and in fact, manufacturing (excluding electrical testing) of "flight" 623C parts has been done by American Microsystems Inc. (AMI).

The particular process used involves the application of ion-implantation to produce depletion resistors and "low-threshold" enhancement transistors on the surface of a "111-" oriented, N-type silicon wafer. Six levels of photo-masking are used to control P⁺ diffusion, gate-oxide regions, oxide-contact-hole regions, metal deposition, depletion-resistor implant, and protective-oxide removal, respectively. The photo-tools are prepared using a computer-aided microcircuit artwork system (CAMAS), which in turn controls an automated pattern generator. The smaller aluminum lines shown in figure 1 are 7.5- μ m wide, while the chip itself is approximately 3-mm square. Chips are connected to the flat package using thermo-compression bonded, 25- μ m gold wire.

A more detailed description of PMOS processes may be found in Reference 1. A short description of some related circuits designed at GSFC is included in Appendix A.

USER INTERFACE INFORMATION

The 623 devices are supplied in a 22-lead round flatpack (see figure 3) which is usually shipped in a plastic carrier to facilitate handling and testing.

As with all MOS devices, precautions should be taken to avoid the possibility of static electric damage in handling and installation. To reduce the possibility of damage, a static protection circuit (figure 4) is used on each input lead to protect the gate oxide. The voltage on any pin, measured relative to pin 1, must therefore be maintained between +0.5V and -20V to prevent damage to the device. The bottom of the case is electrically connected to pin 1.

The 623 is designed to draw a typical power supply current of 1.2 mA on pin 20 (-V1) and 15 μ A on pin 21 (-V2). Because these currents are relatively insensitive to power supply voltage in the operating range of -6 to -12 volts for -V1, power for a 10-V supply is typically 12 mW.

The timing of the data interface between the 623 and the host instrument is shown in figure 5. The convert signal (pin 15) must be high for a minimum of 5 ms during which counting is inhibited. The clock signal must be low for a minimum of 10 μ s before and after the

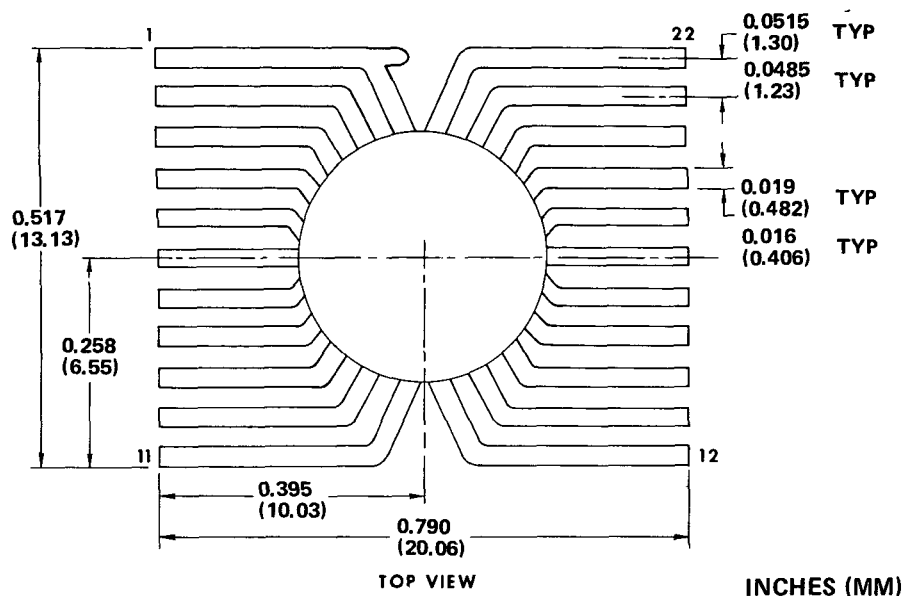


Figure 3. 22-lead flatpack.

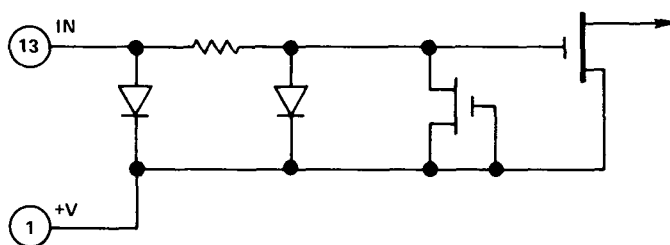


Figure 4. Static protection device

falling edge of the convert signal. The most significant bit of Y will appear at pin 22 within 10 μ s after the falling edge of the convert pulse (if tri-state signals I1 and I2 are both positive). The serial output changes state (and the serial input is sampled) at the falling edge of the clock, which should not exceed 100 kHz (square wave). The pulse input signal should not exceed 1 MHz (square wave), should be normally low, and should have a minimum pulse width of 400 ns.

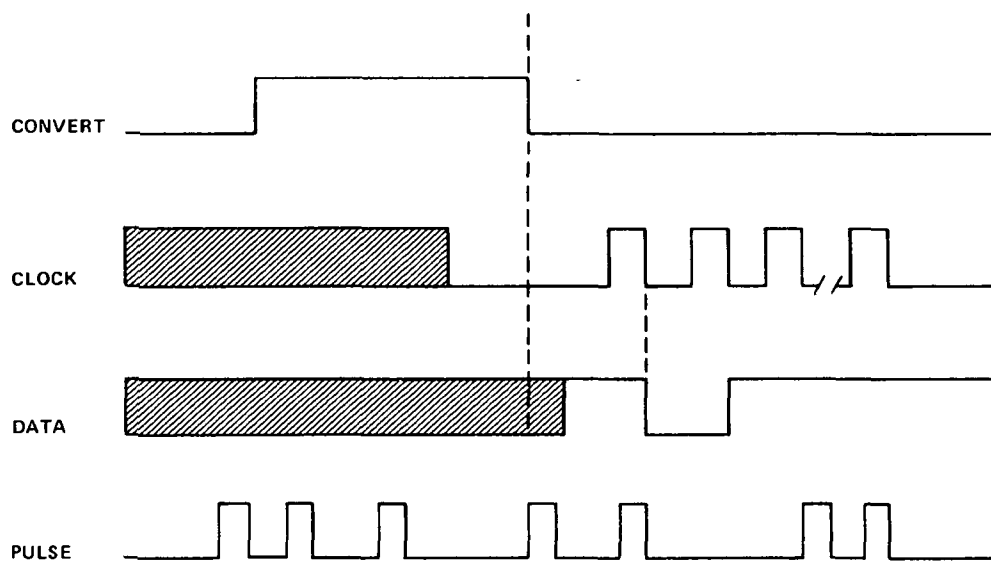


Figure 5. Timing signals.

The threshold or switching point for input signals to the 623 will be between -1 V and -4 V measured relative to pin 1 (+V). As a result, care must be taken that input signals substantially attain the positive rail voltage while not exceeding it by more than 0.5 V. This requirement can cause difficulty, especially with regard to the high-speed pulse input signal.

An overflow-prevention option is available at pin 5. If this pin is connected to one of the input gate terminals, counting can be inhibited at approximately half of full-scale, preventing the possibility of ambiguous data. The pin 5 output does not have a pull-down resistor, so an external resistor of about 100 kilohms is required between pin 5 and pin 20 (-V1).

A two-transistor gate for use in implementing user logic is available at input pins 6 and 8 such that if either pin is low, the output pin 7 is clamped to +V with a resistance of about 2 kilohms.

Parts intended for space flight use are tested by computer-automated equipment and by a printed report generated for each serialized part. An outline of this test and other quality procedures may be found in Appendix B.

DATA CONVERSION ALGORITHMS

The following algorithms are used to recover the original binary count, C , from the telemetered values of X and Y . In the serial data, the value of Y is shifted out first, followed by X . The most significant bit of each is transmitted first.

The algorithms for the 19-bit mode are different from those of the 27-bit mode. In each case the telemetered Y value must be converted to an N value using the appropriate lookup table (tables 2 and 3).

Table 2
Y to N Lookup Table for 19-Bit Mode

Y	N	Y	N	Y	N
0	0	6	14	11	9
1	11	7	13	12	4
2	10	8	8	13	7
3	1	9	3	14	6
4	12	10	2	15	5
5	0				

Table 3
Y to N Lookup Table for 27-Bit Modes

Y	N	Y	N	Y	N	Y	N
0	13	8	21	16	XX	24	5
1	24	9	16	17	8	25	0
2	23	10	15	18	7	26	XX
3	14	11	22	19	XX	27	6
4	25	12	17	20	9	28	1
5	12	13	20	21	XX	29	4
6	11	14	19	22	27	30	3
7	26	15	18	23	10	31	2

In the 19-bit mode, the algorithm is as follows

If $X = 15$ and $Y = 6$, $C = 0$

If $Y = 5$, $C = X + 1$

Otherwise, $C = 1 + (X + 16) \cdot 2^N$

(1)

In the 27- to 12-bit mode

$$\begin{aligned} &\text{If } Y = 22 \text{ and } X = 127, C = 0 \\ &\text{Otherwise, } C = 1 + (X + 128) \cdot 2^{(N-8)} \end{aligned} \quad (2)$$

In the 27-bit modes, certain values of Y should never occur. These are denoted in table 3 by "XX." Fractional parts of a result are discarded.

In computer processing of data produced in the 19-bit mode, it may be more advantageous to look up the result in a table rather than to calculate it using algorithm 1. This information is provided in Appendix C where X and Y are expressed as a single octal number and C is expressed as a decimal number.

The information given by the table or by the algorithms represents the lowest value of input count which would result in the given X and Y values. For example, the table entry (octal), 143, represents an X value of 3 and a Y value of 6 (N = 14). Using either algorithm 1 or Appendix C, the minimum input count is 311297. However, any input count between 311297 and 327680 would result in a code of 143. The mean value of all such input counts is therefore 319489, and for this reason, the user may desire to substitute 16.5 for 16 in algorithm 1 and 128.5 for 128 in algorithm 2 to recover the mean value rather than the lowest value of count.

The maximum count that may be accumulated without overflow is 507904 in the 19-bit mode and 133693440 in the 27-bit mode. If the overflow prevention option is used, counting will be inhibited at approximately half scale (262145 for 19-bit mode, 67108865 for 27-bit mode).

CIRCUIT OPERATION ANALYSIS

Device Physics

The 623 is implemented using only the three circuit elements (active devices, depletion resistors, and capacitors) which can be produced using the monolithic PMOS process. Active devices are enhancement-type P-channel transistors with a nominal threshold voltage (V_T) of approximately -2 V. The current carrying capacity of the transistor (when turned on) is governed by the physical size of the device, which is denoted on the schematic drawings by a channel width-to-length ratio. (For example, a 20:1 device will have half the resistance exhibited by a 10:1 device under a given circumstance.) The resistors are depletion-type P-channel transistors which act as current sources to power the active portion of the circuitry. The current supplied by such a device is a function of physical size. For the GSFC process it is approximately 45 μA for a unity width-to-length ratio. (For example, a 1:10 depletion resistor will supply a current of about 4.5 μA .) MOS capacitors may be made in sizes up to about 10^{-11} farads.

Cell Descriptions

The 623 employs over 1000 devices to implement 40 register flipflops, 2 monostable timing circuits, and a free running clock oscillator as shown in the interconnection diagram (figure 6). Figure 6 references various subcircuits or “cells.” The most important cell is the shifting counter flipflop shown in figure 7 which consists of two latch flipflops interconnected by logic to form the master-slave flipflop configuration. In this case, the logic can be used to configure the flipflop to act as either a counter or a shift register stage. The circuit counts when the signal C is negative and the signals SC and \overline{SC} are positive. For shifting, C is positive and the shift register clocks are applied to SC and \overline{SC} . A high speed version, A, is used in the first 3 bits of the A register; the lower power C version is used elsewhere.

The switch cell S (figure 8) is used to switch between two different signal sources. Source IN is selected when C is positive; source B is selected when C is negative.

The “one-shot” multivibrator of figure 9 is used to generate a fixed length pulse following the positive going edge of an input signal. MOS capacitors and depletion resistors are used to provide the required time delay.

A free running oscillator (figure 10) provides clock waveforms during the conversion process. When I is negative, the clock is inhibited. The clock starts synchronously with the release of the I signal to avoid difficulties with partial clock pulses.

A clock driver (figure 11) provides the necessary two-phase clock signal for shifting the A, X, and Y registers. The “I” input (when negative) forces both phase outputs to be positive.

Assorted small gates and the tri-state output driver are shown in figure 12. Because of the threshold characteristics of the active pull-down device, a separate power supply connection (pin 21) is provided. Unless this supply is several volts more negative than pin 20, the serial output will not be a “rail-to-rail” signal but will stop short of the negative supply. If the reduced logic swing is acceptable, pin 20 and pin 21 can be connected to the same supply.

Figure 13 shows details of two large gate circuits. Note that the gate symbology on figure 6 is for negative true signals.

Sequence of Operations

The sequence of operations is shown in figure 14. At the leading edge of the convert pulse, counting of the A register is inhibited, the X register is reset to zeroes, and the Y register is reset to ones. The counter is allowed to settle until the end of the OS1 signal. A is then reoriented to shifting mode and the A and X registers are shifted to the right until stopped by the conversion control logic. During shifting, ones are introduced into the left end of the A register and the Y register is incremented for each shift. In the 27-bit modes, shifting is stopped when a one is shifted into flipflop X35. The next seven most significant bits of the count are then in the X register. If A were all ones, 8 shifts would have occurred, if A were all zeroes, 35 shifts would occur before shifting was halted. In the 19-bit mode, shifting

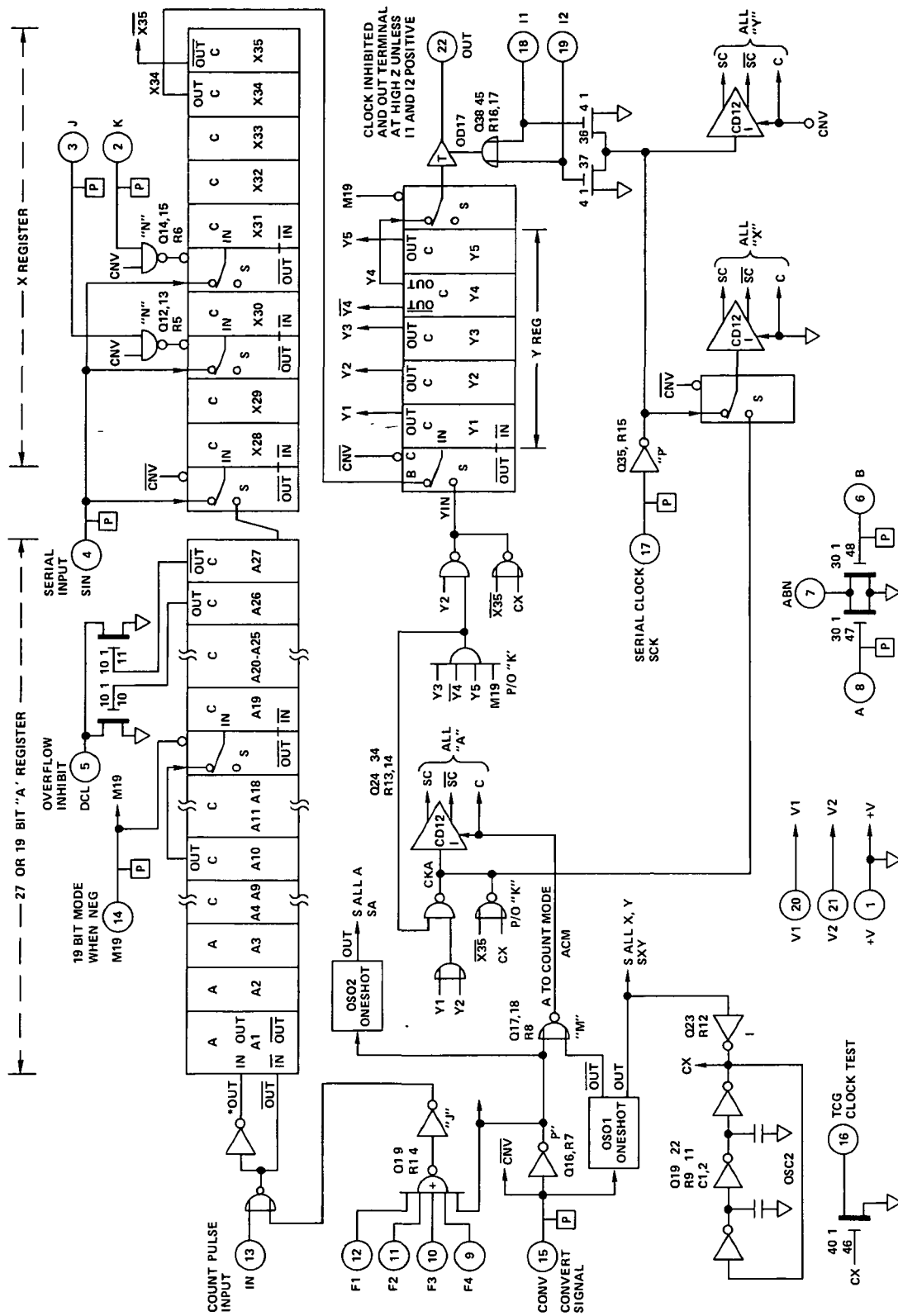


Figure 6 Interconnection diagram.

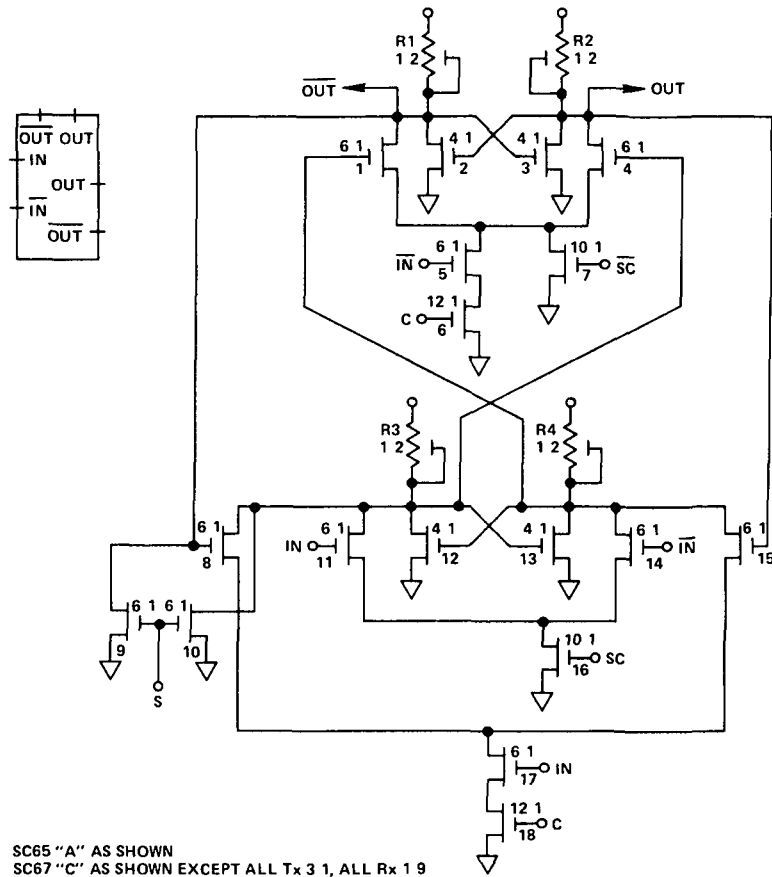


Figure 7. Shifting counter register

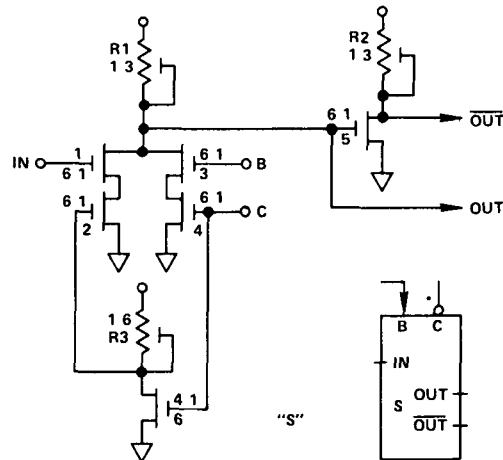


Figure 8 Switch cell SW23.

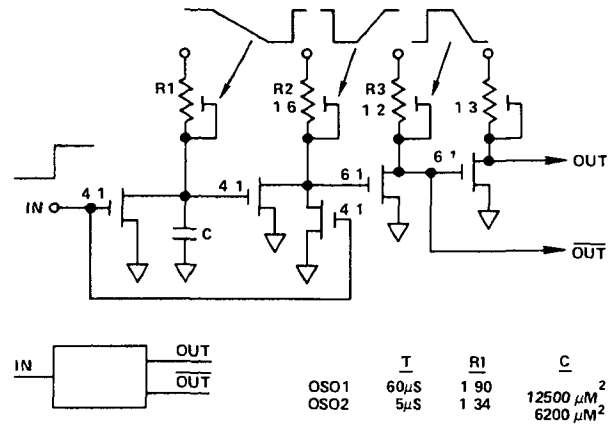


Figure 9 Multivibrator cell.

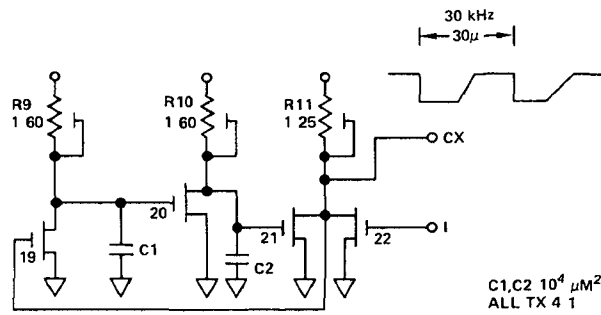


Figure 10 Clock oscillator, cell OSC2

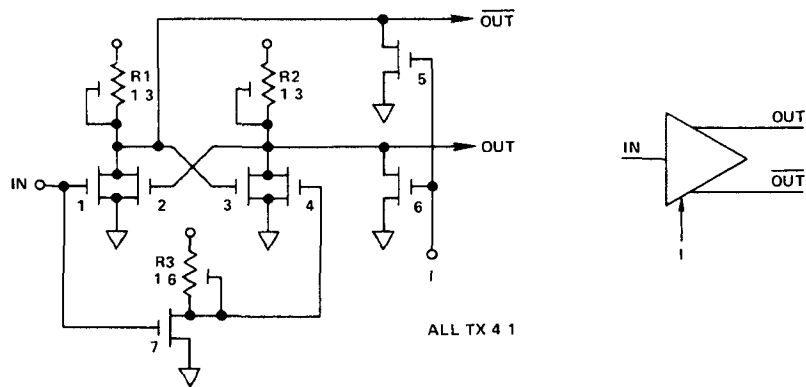


Figure 11. Clock driver, cell CD12

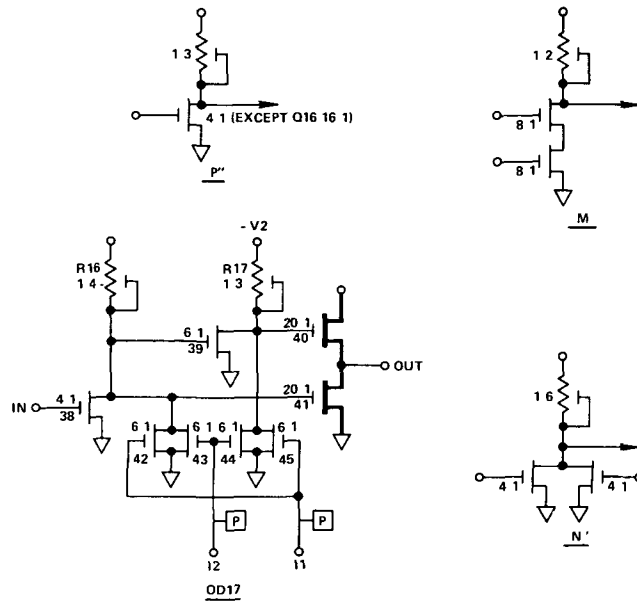


Figure 12. Output driver and miscellaneous cells

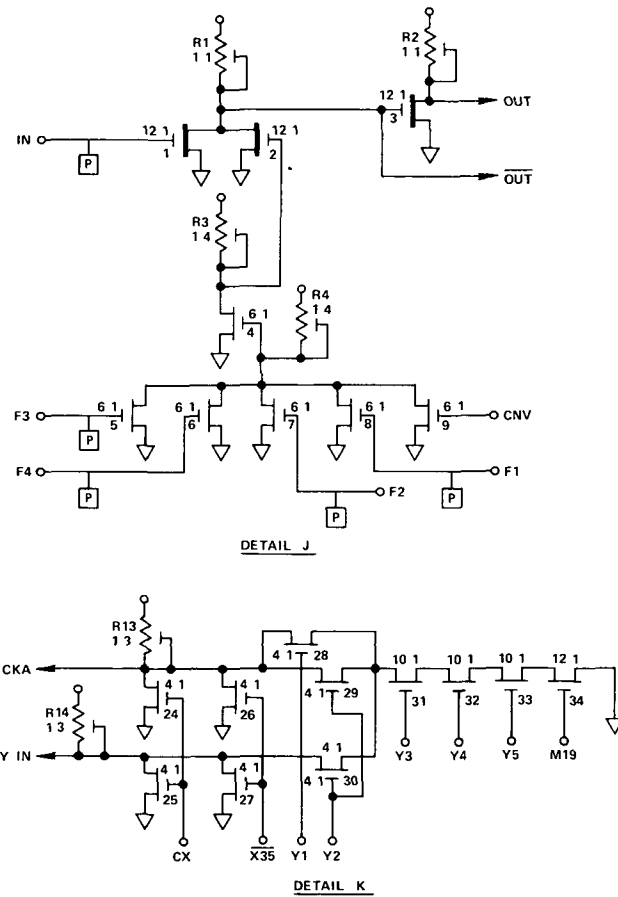


Figure 13 Logic gates

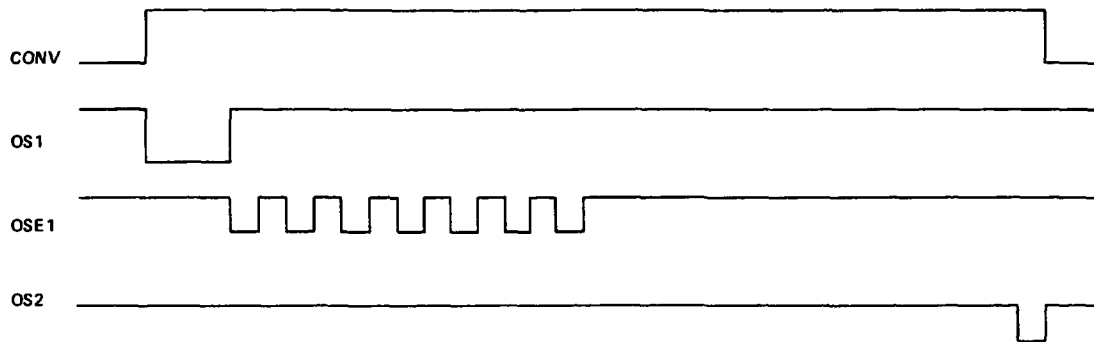


Figure 14 Internal timing for 623.

is stopped when X35 contains a one, or when the least significant 4 bits of the count are in the most significant 4-bit positions of the X register (22 shifts). To eliminate ambiguity between these two cases, the Y register is incremented an additional time, if X35 is a zero after 22 shifts. Following the falling edge of the convert pulse, the A register is reset to ones and counting is reenabled. The X and Y register are configured for shifting with lengths controlled by the mode control signals and with clock inputs connected to pin 17. Data can be shifted out at any time prior to the next convert signal.

Radiation Resistance

Ionizing radiation (such as that encountered in a planetary trapped-radiation belt) has a damaging effect on semiconductor devices. For PMOS, the primary effect is the introduction of positive charge sites in the gate oxide which tends to reduce the current in the depletion resistors, eventually to zero. Since the speed of the circuit is dependent on current, radiation failure occurs when the device speed is reduced below that required for a particular application. Radiation tests have been performed on the 623 by the National Oceanic and Atmospheric Administration (NOAA) in connection with a TIROS-N instrument*, where the failure criterion was the inability to count 1 MHz pulses. Twelve 623 flight parts were irradiated with Cobalt-60 and failed at exposures of between 9400 and 23500 (average 16000) rads (silicon).

Typically, the 623 will operate properly on initial testing for pulses between 2 and 3 MHz. If the devices had been screened to eliminate those with an initial counting speed of less than 2.5 MHz (half of the samples), the first failure would have been at 13500 rads, and the average failure dose would have been 18600 rads. Similar results would have been obtained if the half of the 12 samples with lower power had been eliminated. (The samples ranged between 9.8 and 12.0 mW.)

*R. A. Seale, *P-MOS 623C Compression Counter Radiation Test Results*, Space Environment Laboratory, NOAA, Boulder, Co., April 1976.

CONCLUSION

The 623 circuit performs pulse accumulation and count compression functions in a single monolithic unit. When used to replace conventional, MSI implemented, logarithmic compressors in space physics experiments, this circuit can result in substantial reductions in cost, weight, and volume. The design permits easy interfacing with contemporary spacecraft telemetry systems.

REFERENCE

1. American Microsystems Inc., *MOS Integrated Circuits*, Van Nostrand Reinhold, 1972.

APPENDIX A

RELATED GSFC PMOS CIRCUITS

Brief descriptions of some related PMOS circuits currently being developed at GSFC are presented below.

The 632 (figure A-1) is in the design phase and consists of four 19-bit floating point accumulators with serial output registers connected in series. This unit will involve 139 flipflops and approximately 3100 devices on a chip measuring 5.2 mm by 5.6 mm, mounted in a 28-lead flatpack. Power requirement is expected to be approximately 30 mW, and operation is similar to the 623.

The 633 (figure A-2) is in the production phase for use on Solar Maximum Mission (SMM) and International Sun-Earth Explorer (ISEE) spacecraft. It consists of two binary counters parallel-coupled to two shift registers and is used in cases where linear rather than floating point accumulation is desired. The counters and shift registers can be electrically programmed to any of 6 different lengths, up to 24 bits. This circuit has 101 flipflops on a chip 4.6 by 4.3 mm, mounted in a 28-lead flat package.

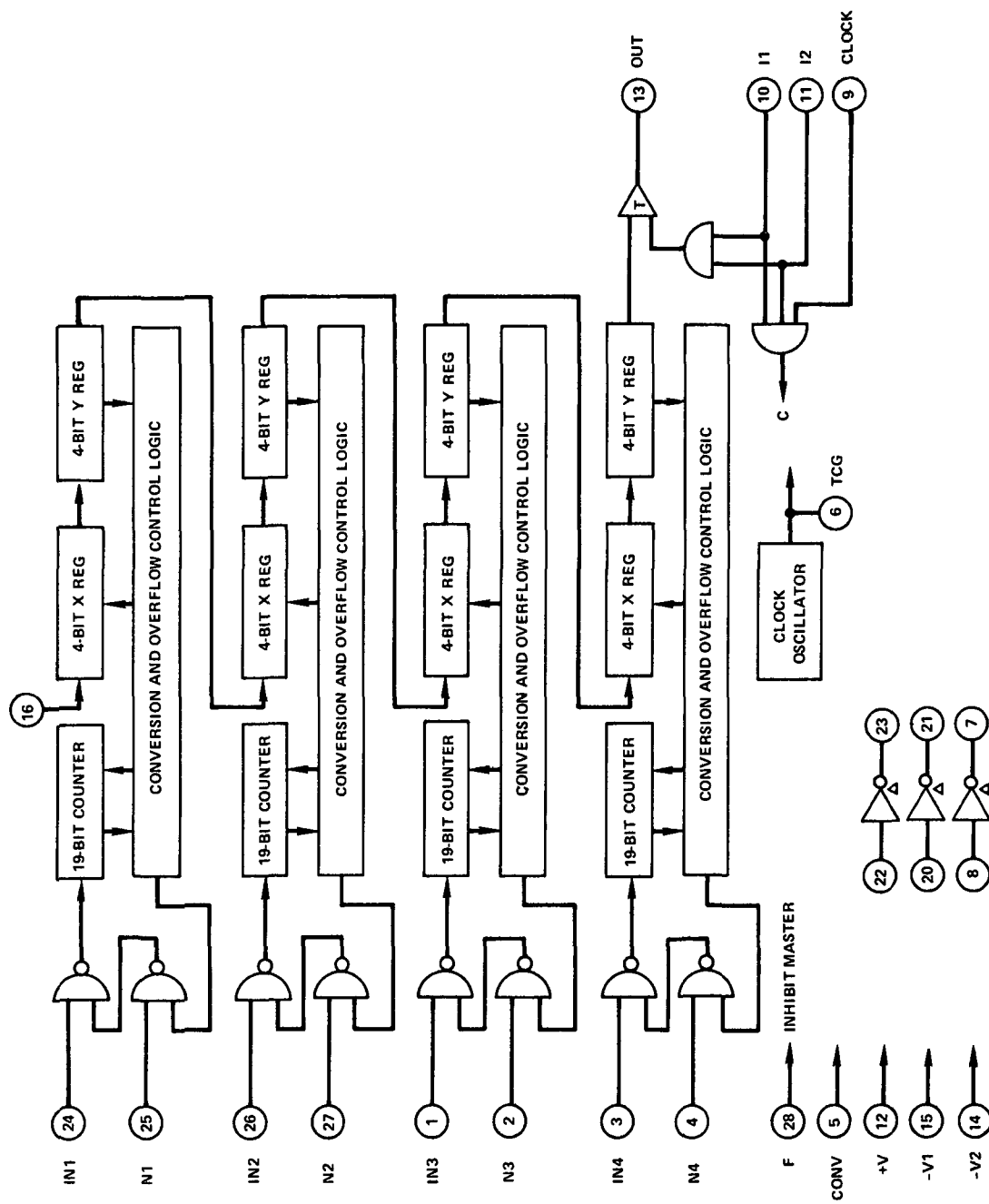


Figure A-1. GSFC type 632 quad 19- to 8-bit floating point processor.

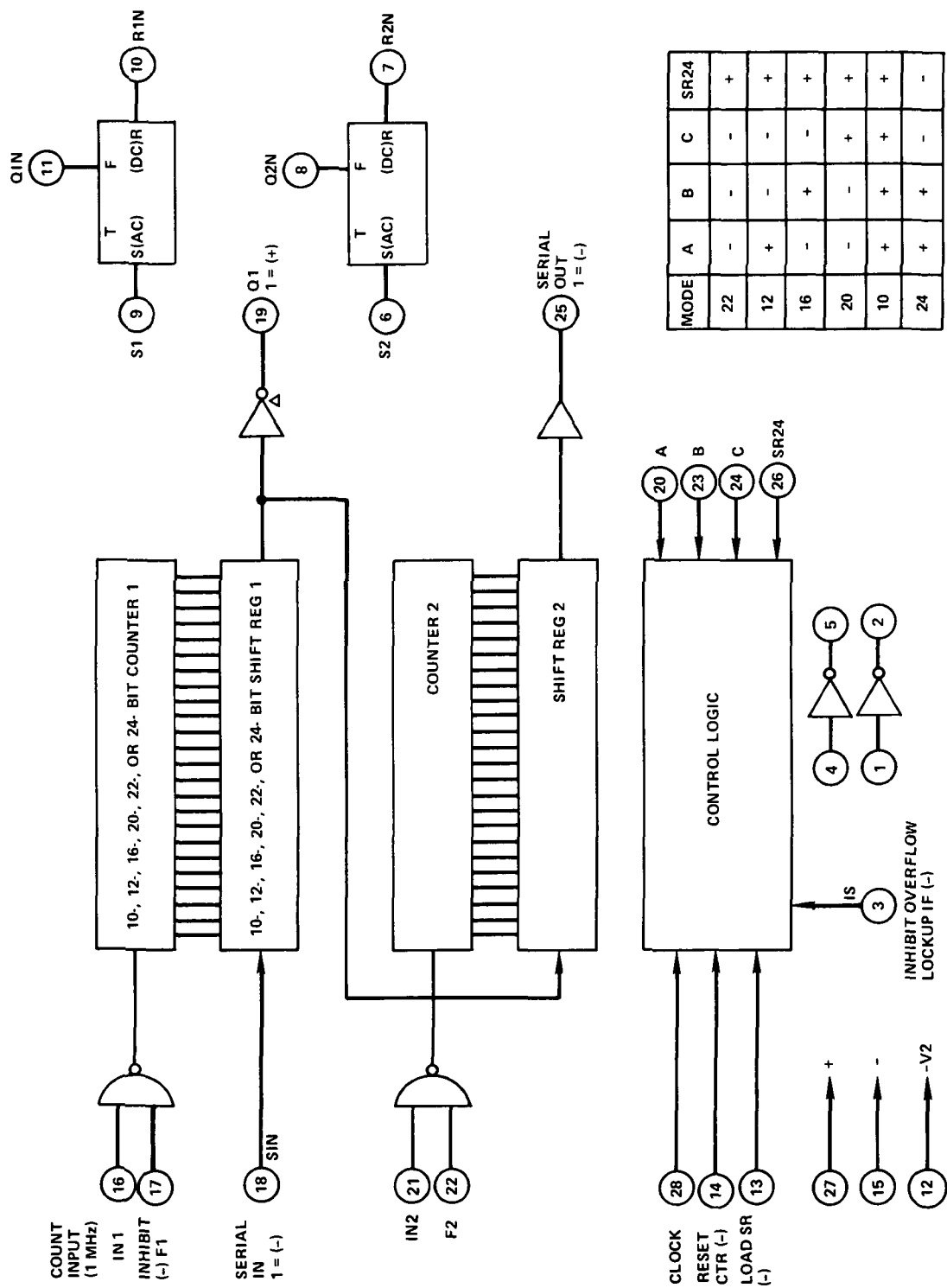


Figure A-2. GSFC type 633 dual counter register.

APPENDIX B

ACCEPTANCE TEST PROCEDURE

The following is keyed to the corresponding section of the serialized test report.

1. Module Type 6231 TIROS-N test at 10 V except as indicated below. International Sun-Earth Explorer test sequence 623 is identical except the nominal voltage level is 7.75 V and the functional tests are executed at 9.75, 7.75, and 5.75 V.
2. Bond Test Lead continuity is checked by applying +10 V through 100 kilohms and accepting only 0.5 to 0.9 V.
3. Breakdown Test Output and power supply pins are measured for less than 10 μ A current when connected to -30 V.
4. Saturation Test Load resistors are connected to chip outputs, and the resulting output voltages and calculated resistances are listed. The acceptance levels are 4.5 kilohms max.
5. Threshold Test The serial input line is measured to determine minimum and maximum position of the one/zero threshold relative to +V.
6. Input Leakage Test All input pins are screened for 10^{-5} μ A maximum leakage at -30 V.
7. Power Consumption Power at nominal voltage is measured.
8. Functional Tests Unit is tested at 12 V, 10 V, and 7.75 V.
 - a. Unit is tested for shifting at 100 kilobits/second.
 - b. The inhibit lines are tested.
 - c. Proper conversion at 1-kHz-count input rate is verified for 0, 1, and 17 counts in the 12-bit mode, 0, 1, and 19 counts in the 8-bit mode, and zero counts in the 10-bit mode.
 - d. The freeze inputs are tested.
 - e. The aux gate is tested.
 - f. High speed (2 MHz) counting and conversion are checked for 4, 7, 13, 33, 513, and 132097 counts in the 12-bit mode.
 - g. The DCL overflow signal is checked (507904 counts).

Other quality procedures performed on flight units include:

- a) Scanning electron microscope inspection of sample chips
- b) 100-percent prebond optical inspection
- c) 100-percent preseal visual
- d) Temperature cycle 5 times - (65° to +150°C)
- e) Centrifuge 20,000 G
- f) Fine leak test (5×10^{-8} cc/s Helium)
- g) Gross leak test
- h) 100-percent final visual
- i) Power on burn-in for 100 hours at 125°C

APPENDIX C **623 OCTAL CODE TO COUNTS CONVERSION TABLE** **19-BIT MODE**

0	17	1	18	2	19	3	20	4	21	5	22	6	23	7	24
10	25	11	26	12	27	13	28	14	29	15	30	16	31	17	32
20	32769	21	34817	22	36365	23	38913	24	40361	25	43009	26	45057	27	47105
30	49153	31	51201	32	53249	33	55297	34	57345	35	59393	36	61441	37	63489
40	16335	41	17409	42	18433	43	19457	44	20481	45	21505	46	22529	47	23553
50	24577	51	25601	52	26625	53	27649	54	28673	55	29697	56	30721	57	31745
60	33	61	35	62	37	63	39	64	41	65	43	66	45	67	47
70	49	71	51	72	53	73	55	74	57	75	59	76	61	77	63
80	55537	81	69633	82	73729	83	77825	84	81921	85	86017	86	90113	87	94209
90	98205	91	102401	92	106497	93	110593	94	114689	95	118785	96	122881	97	126977
100	1	101	2	102	3	103	4	104	5	105	6	106	7	107	8
110	130	111	10	112	11	113	12	114	13	115	14	116	15	117	15
120	262145	121	278529	122	294913	123	311297	124	327681	125	344065	126	360449	127	376833
130	393217	131	409601	132	425985	133	442369	134	458753	135	475137	136	491521	137	507905
140	131073	141	139265	142	147457	143	155649	144	163841	145	172033	146	180225	147	188417
150	176609	151	204801	152	212993	153	221185	154	229377	155	237569	156	245761	157	253953
160	4097	161	4353	162	4609	163	4865	164	5121	165	5377	166	5633	167	5889
170	6145	171	6401	172	6657	173	6913	174	7169	175	7425	176	7681	177	7937
180	129	181	137	182	145	183	153	184	161	185	169	186	177	187	185
190	193	191	201	192	209	193	217	194	225	195	233	196	241	197	249
200	65	201	63	202	73	203	77	204	81	205	85	206	89	207	93
210	97	211	101	212	105	213	109	214	113	215	117	216	121	217	125
220	8193	221	8705	222	9217	223	9729	224	10241	225	10753	226	11265	227	11777
230	12239	231	12801	232	13313	233	13825	234	14337	235	14849	236	15361	237	15873
240	257	241	273	242	289	243	305	244	321	245	337	246	353	247	369
250	385	251	401	252	417	253	433	254	449	255	465	256	481	257	497
260	2049	261	2177	262	2305	263	2433	264	2561	265	2689	266	2817	267	2945
270	3073	271	3201	272	3329	273	3457	274	3585	275	3713	276	3841	277	3969
280	1025	281	1089	282	1153	283	1217	284	1281	285	1345	286	1409	287	1473
290	1537	291	1601	292	1665	293	1729	294	1793	295	1857	296	1921	297	1985
300	513	301	545	302	577	303	609	304	641	305	673	306	705	307	737
310	769	311	801	312	833	313	865	314	897	315	929	316	961	317	993



POSTMASTER

If Undeliverable (Section 158
Postal Manual) Do Not Return

"The aeronautical and space activities of the United States shall be conducted so as to contribute . . . to the expansion of human knowledge of phenomena in the atmosphere and space. The Administration shall provide for the widest practicable and appropriate dissemination of information concerning its activities and the results thereof"

—NATIONAL AERONAUTICS AND SPACE ACT OF 1958

NASA SCIENTIFIC AND TECHNICAL PUBLICATIONS

TECHNICAL REPORTS Scientific and technical information considered important, complete, and a lasting contribution to existing knowledge

TECHNICAL NOTES Information less broad in scope but nevertheless of importance as a contribution to existing knowledge

TECHNICAL MEMORANDUMS Information receiving limited distribution because of preliminary data, security classification, or other reasons. Also includes conference proceedings with either limited or unlimited distribution.

CONTRACTOR REPORTS Scientific and technical information generated under a NASA contract or grant and considered an important contribution to existing knowledge

TECHNICAL TRANSLATIONS Information published in a foreign language considered to merit NASA distribution in English

SPECIAL PUBLICATIONS Information derived from or of value to NASA activities. Publications include final reports of major projects, monographs, data compilations, handbooks, sourcebooks, and special bibliographies

TECHNOLOGY UTILIZATION PUBLICATIONS Information on technology used by NASA that may be of particular interest in commercial and other non-aerospace applications. Publications include Tech Briefs, Technology Utilization Reports and Technology Surveys

Details on the availability of these publications may be obtained from:

SCIENTIFIC AND TECHNICAL INFORMATION OFFICE

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Washington, D.C. 20546